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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MISIURA, BRIAN THOMAS	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,171	MADUKKARUMUKUMANA ET AL.	
	Examiner	Art Unit	
	Brian T. Misiura	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,10,14-16,23,27-29,31,33,36,37,40-42,44,46 and 49-51* is/are rejected.

7)☒ Claim(s) *4-9,11-13,17-22,24-26,30,32,34,35,38,39,43,45,47,48 and 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 27, 28, 37, 40, 41, 50, 51 rejected under 35 U.S.C. 102(b) as being anticipated by Takagi, U.S. Patent No. 5,371,857.

Per claim 27, Takagi discloses:

- a plurality of processors (figure 1, numerals IP0, IP1, IOP) to execute a plurality of virtual machines (figure 1, numerals 8-9, column 7 lines 16-31) having virtual machine identifiers (column 1 lines 52-61, column 7 lines 16-31)
- an integrated circuit to steer interrupts to the processor utilizing, at least in part, the virtual machine interrupts (column 7 lines 16-31, figure 1, (IP0 forwards the interrupt request, and a processor can be considered an integrated circuit)).

Per claim 28, Takagi discloses wherein each processor is capable of: communicating, to the integrated circuit, the virtual machine identifier of the virtual machine that the processor is currently executing (column 7, lines 16-31, figure 1).

Per claim 37, Takagi discloses each processor includes a memory element to store the virtual machine identifier of the virtual machine that is currently being executed (column 7 lines 47-61, figure 1, numerals 53 and 63).

Per claim 40: Takagi discloses a system comprising:

- a plurality of processors (figure 1, numerals IP0, IP1, IOP) to execute a plurality of virtual machines (figure 1, numerals 8-9, column 7 lines 16-31) having virtual machine identifiers (column 1 lines 52-61, column 7 lines 16-31)

- at least one interrupt generating device to transmit an interrupt having a virtual machine identifier (column 7 lines 16-31, figure 1, (IP0 can be considered the device that generates the interrupt))

- an integrated circuit to steer interrupts to the processor utilizing, at least in part, the virtual machine interrupts (column 7 lines 16-31, figure 1, (IP0 forwards the interrupt request, and a processor can be considered an integrated circuit)).

Per claim 41, please refer to the rejection made above for claim 28.

Per claim 50, please refer to the rejection made above for claim 37.

Per claim 51: Takagi discloses a system wherein the interrupt generating device is capable of:

- being exclusively used by a single virtual machine(column 7 lines 16-31, figure 1, IP0 is the interrupt generating device, and VM0 is the single virtual machine));

- receiving the virtual machine identifier of the virtual machine that has exclusive use of the device (column 7 lines 16-31, figure 1);

- and the interrupt generating device includes a memory element to store the virtual machine identifier (column 7 lines 47-61, figure 1, numerals 53 and 63).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1-2, 14-15, 31, 33, 44, 46 rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi, U.S. Patent No. 5,371,857, in view of Narad, U.S. Patent No. 5,560,019.

Per claim 1, Takagi discloses:

- associating a virtual machine (figure 1, numerals 8-9) with a processor (figure 1, numerals IP0, IP1, IOP) utilizing a virtual machine identifier (column 1 lines 52-61);
- receiving an interrupt (column 6, lines 48-57, figure 1);
- determining if the interrupt is associated with a virtual machine identifier (column 1 lines 52-61) that is associated with one or more processors (column 7, lines 6-31);

Takagi does not disclose routing the interrupt to the matching processor(s).

- However, Narad discloses routing the interrupt to the matching processor(s) (Narad, column 5 lines 59-65, column 6 lines 1-30, figure 2).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Narad into the system of Takagi to provide the system with an efficient interrupt servicing method.

- The modification would have been obvious because one having ordinary skill in the art would want to achieve a system with an efficient interrupt servicing method (Narad, column 3, lines 25-28).

Per claim 2, Takagi discloses:

- determining if the interrupt is associated with a virtual machine identifier (column 1 lines 52-61);
- determining if the virtual machine identifier is associated with one or more processors (column 7, lines 6-31).

Per claims 14 and 15, with the exception of the limitation of "a machine accessible medium having a plurality of machine accessible instructions, wherein when the instructions are executed, the instructions provide for:", the limitations of these claims read identical to those of claims 1 and 2. In order to avoid being redundant, the explanation of rejection regarding claims 14 and 15 will be referenced back to explanation of claims 1 and 2.

Per claim 14: Takagi discloses a machine accessible medium having a plurality of machine accessible instructions (Takagi, column 6, lines 35-48, figure 1). Also, please refer back to the above explanation of claim 1

Per claim 15, please refer to the above explanation of claim 2.

Per claim 31, Takagi discloses

- receiving an interrupt (column 6, lines 48-57, figure 1);
- determining if the interrupt is associated with a virtual machine identifier (column 1 lines 52-61) that is associated with one or more processors (column 7, lines 6-31);

Takagi does not disclose routing the interrupt to the matching processor(s).

- However, Narad discloses routing the interrupt to the matching processor(s) (Narad, column 5 lines 59-65, column 6 lines 1-30, and figure 2).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Narad into the system of Takagi to provide the system with an efficient interrupt servicing method.

- The modification would have been obvious because one having ordinary skill in the art would want to achieve a system with an efficient interrupt servicing method (Narad, column 3, lines 25-28).

Per claim 33, Takagi discloses:

- determining if the interrupt is associated with a virtual machine identifier (column 1 lines 52-61);
- determining if the virtual machine identifier is associated with one or more processors (column 7, lines 6-31).

Per claim 44, please refer to the rejection made above for claim 31.

Per claim 46, please refer to the rejection made above for claim 33.

3. Claims 3, 10, 16, 23, 36, 49 rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi, U.S. Patent No. 5,371,857, in view of Narad, U.S. Patent No. 5,560,019, further in view of Qureshi et al, U.S. Patent No. 5,892,956.

Per claim 3, both Takagi and Narad do not disclose if the interrupt is not associated with a virtual machine identifier, utilizing a virtual control block to steer the interrupt to the appropriate processor.

- However, Qureshi discloses if the interrupt is not associated with a virtual machine identifier, utilizing a virtual control block to steer the interrupt to the appropriate processor (Qureshi, column 7, lines 61-67, column 8 lines 1-2, figure 3).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Qureshi into the system of Takagi and Narad have an interrupt steering mechanism to send interrupts that don't have a predetermined destination.

- The modification would have been obvious because one having ordinary skill in the art would want to have an interrupt steering mechanism in the event an interrupt does not include a specified destination (Qureshi, column 7, lines 61-67, column 8 lines 1-2, figure 3).

Per claim 10: Takagi discloses the virtual machine identifier is associated with multiple processors (column 7, lines 6-31)

Takagi does not disclose routing the interrupt to the associated processor with the lowest task priority.

- However, Qureshi discloses routing the interrupt to the associated processor with the lowest task priority (Qureshi, column 8 lines 2-6, column 2 lines 57-61).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Qureshi into the system of Takagi and Narad in order to utilize the systems resources.

- The modification would have been obvious because one having ordinary skill in the art would want to utilize the systems resources (Qureshi, column 8 lines 2-6, column 2 lines 57-61).

Per claims 16 and 23, with the exception of the limitation of "a machine accessible medium having a plurality of machine accessible instructions, wherein when the instructions are executed, the instructions provide for:", the limitations of these claims read identical to those of claims 3 and 10. In order to avoid being redundant, the explanation of rejection regarding claims 16 and 23 will be referenced back to explanation of claims 3 and 10.

Per claim 16, please refer to the above explanation of claim 3.

Per claim 23, please refer to the above explanation of claim 10.

Per claim 36: Takagi discloses if the virtual machine identifier is associated with multiple processors

Takagi does not disclose routing the interrupt to the associated processor with the lowest task priority.

- However, Qureshi discloses routing the interrupt to the associated processor with the lowest task priority (Qureshi, column 8 lines 2-6, column 2 lines 57-61).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Qureshi into the system of Takagi and Narad in order to have utilized the systems resources.

- The modification would have been obvious because one having ordinary skill in the art would want to utilize the systems resources (Qureshi, column 8 lines 2-6, column 2 lines 57-61).

Per claim 49, please refer to the rejection made above for claim 36.

4. Claims 29 and 42 rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi, U.S. Patent No. 5,371,857, in view of Ohtsuki, U.S. Patent No. 5,101,346.

Per claim 29, Takagi does not disclose wherein the integrated circuit is capable of associating each processor with a virtual machine identifier, and the associations are stored in a participant table.

- However, Ohtsuki discloses wherein the integrated circuit is capable of associating each processor with a virtual machine identifier, and the associations are stored in a participant table (column 3 lines 66-68, column 4 lines 7, figures 3A and 3B).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Ohtsuki into the system of Takagi to provide a structure for mapping virtual machine id's to processors.

- The modification would have been obvious because one having ordinary skill in the art would want to provide a structure for mapping virtual machine id's to processors (column 3 lines 66-68, column 4 lines 7, figures 3A and 3B).

Per claim 42, please refer to the rejection made above for claim 29.

Allowable Subject Matter

Claims 4-9, 11-13, 17-22, 24-26, 30, 32, 34, 35, 38, 39, 43, 45, 47, 48, 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BTM

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
10/31/05